

[illegible]

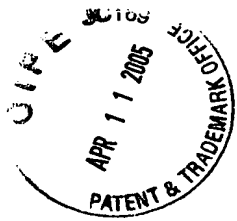


FIG. 2A

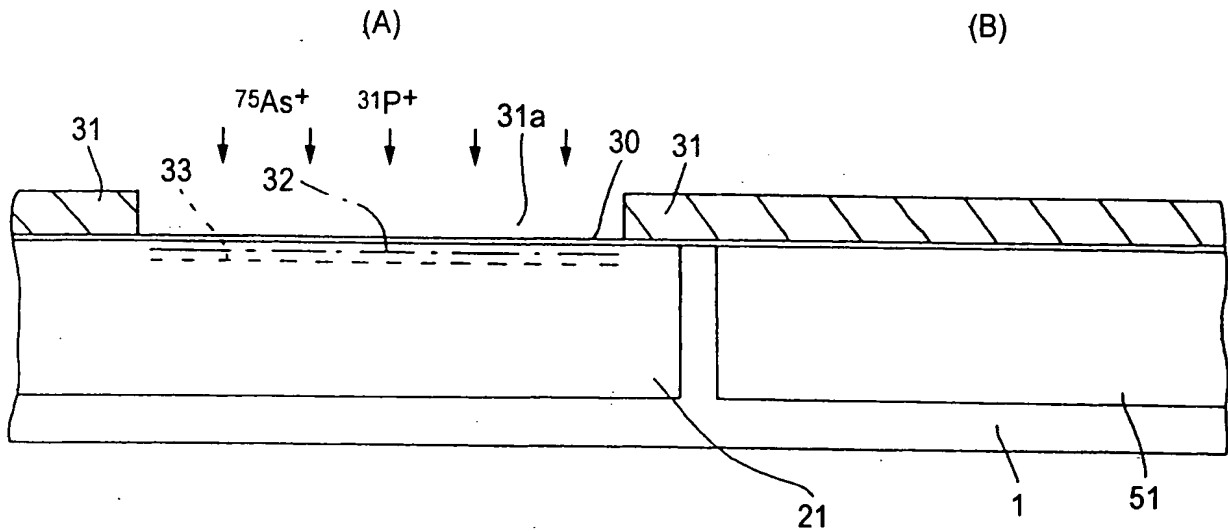
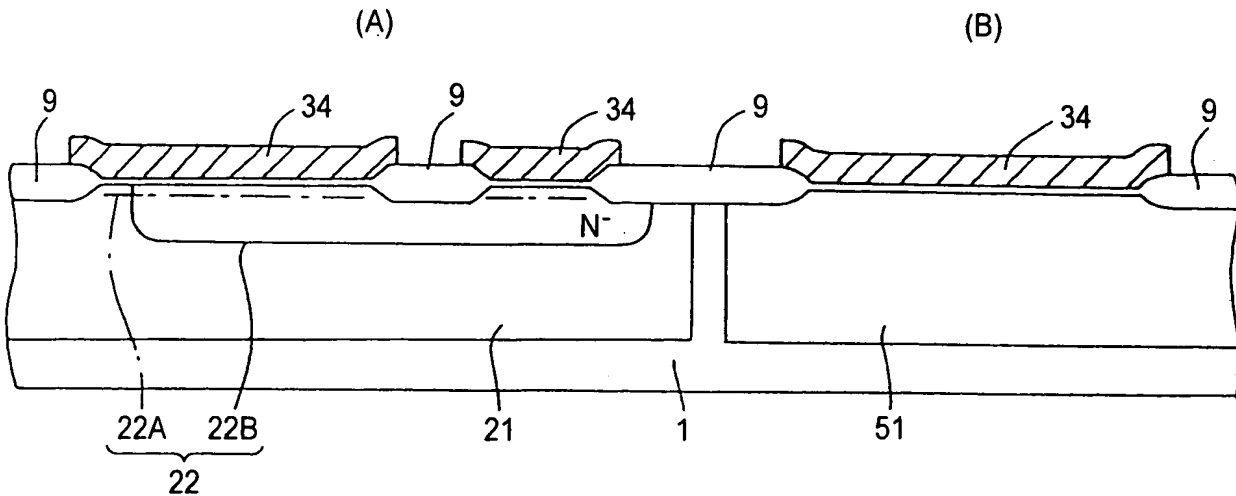


FIG. 2B



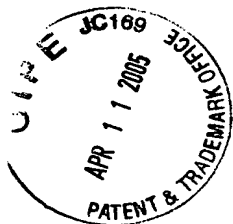


FIG. 3A

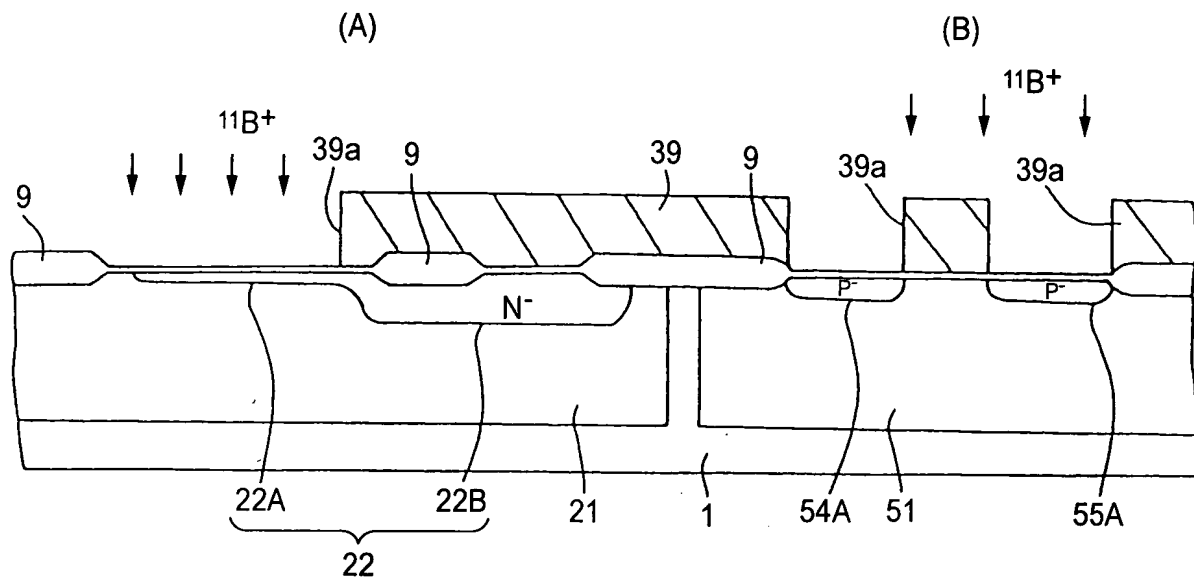
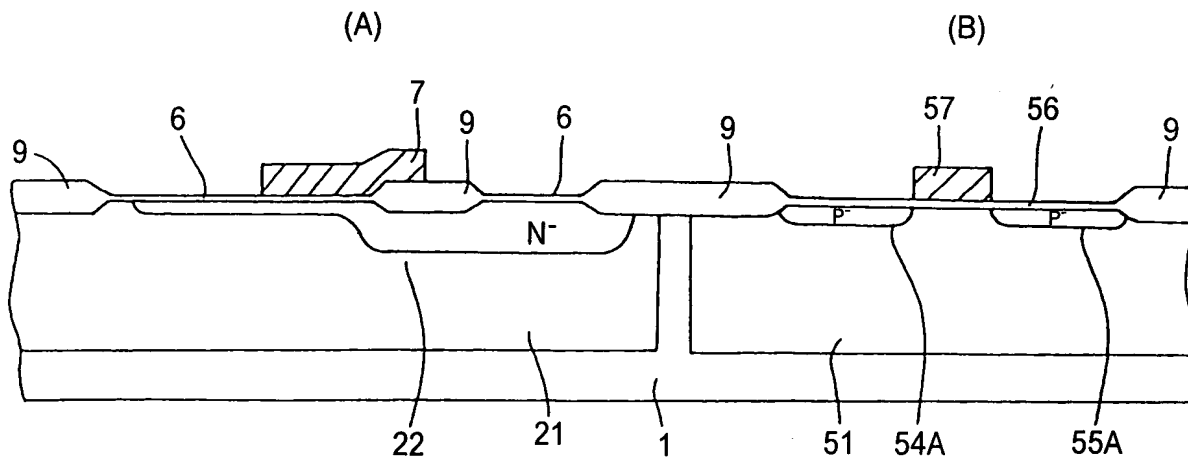


FIG. 3B



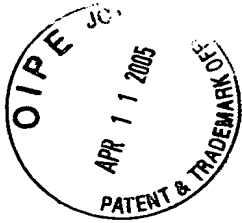


FIG. 4A

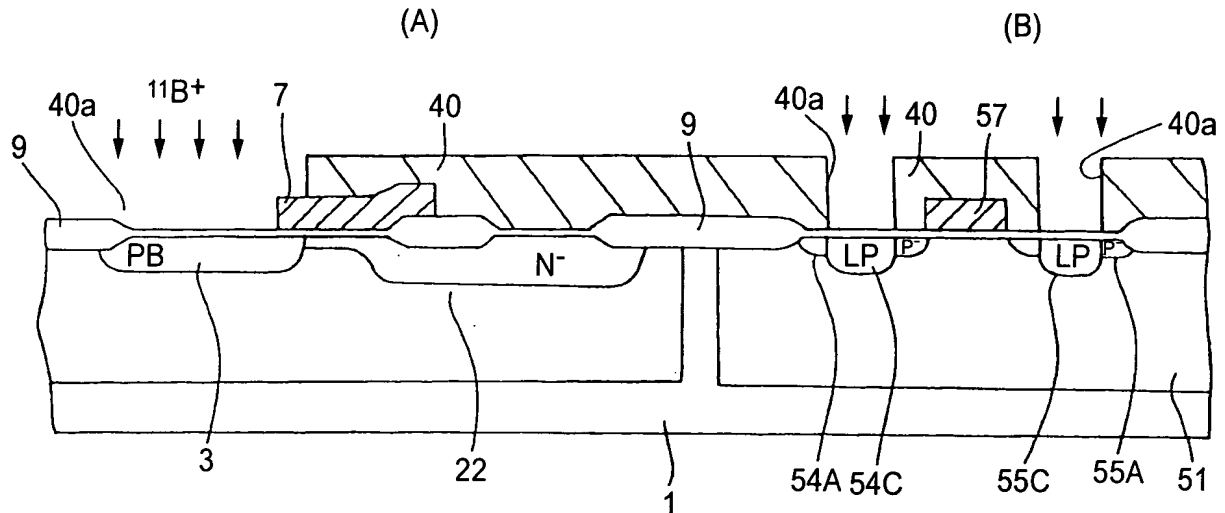
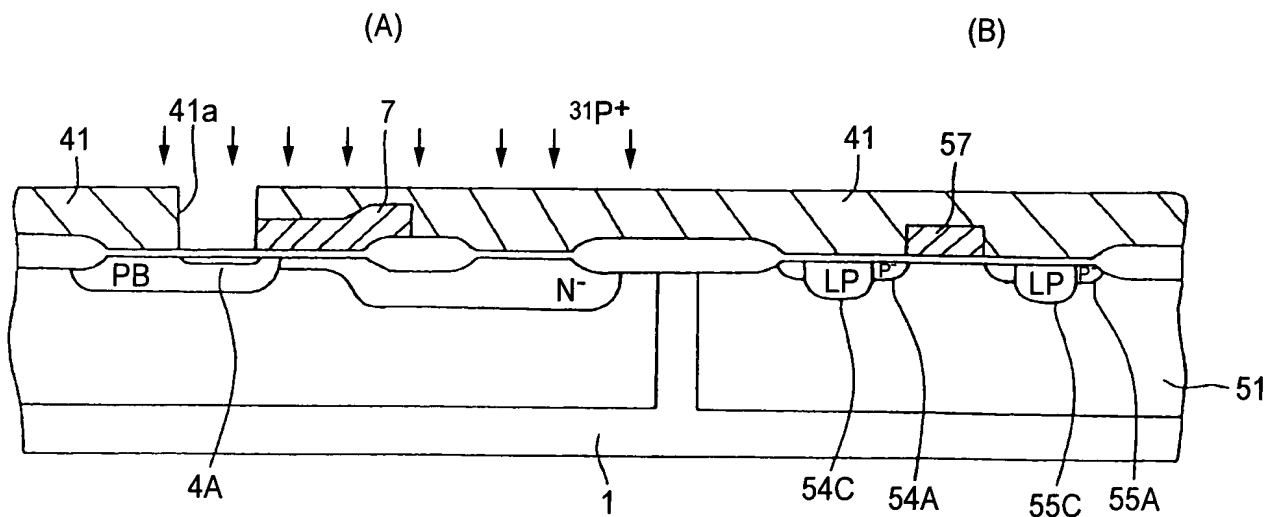


FIG. 4B



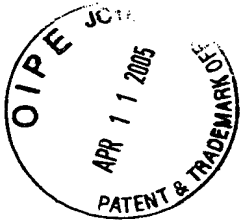


FIG. 5A

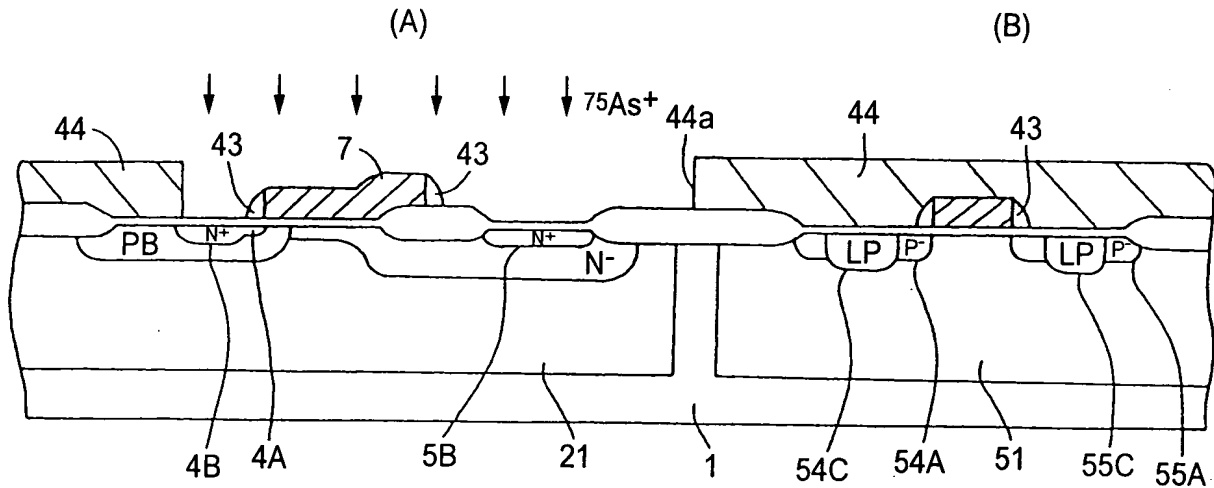
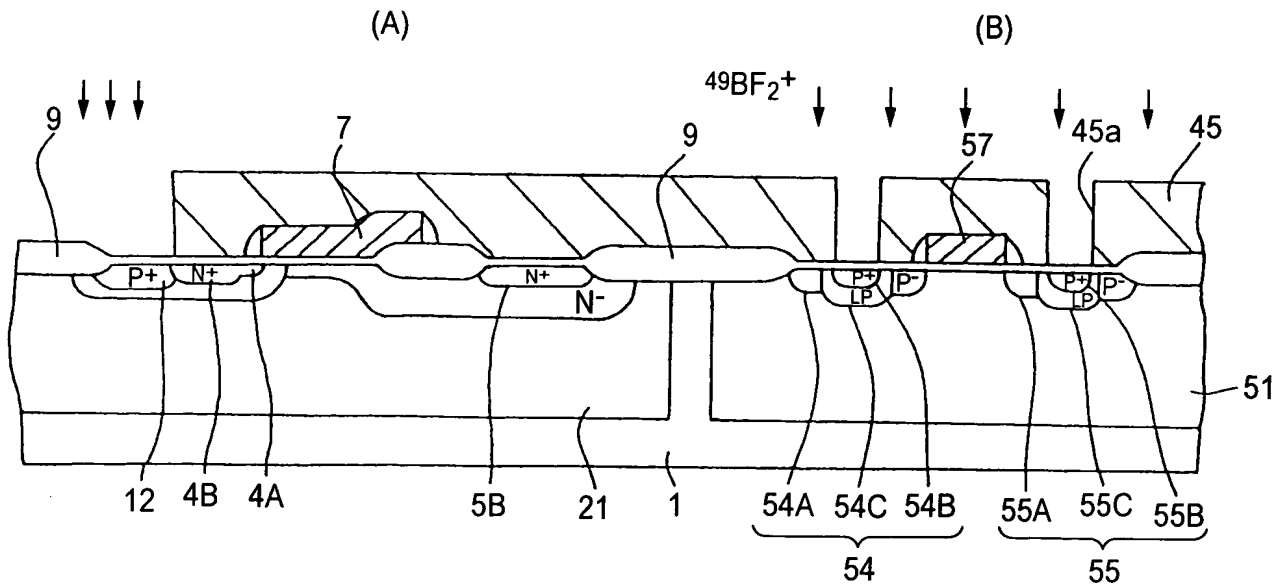


FIG. 5B



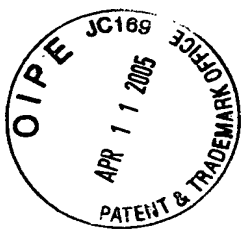
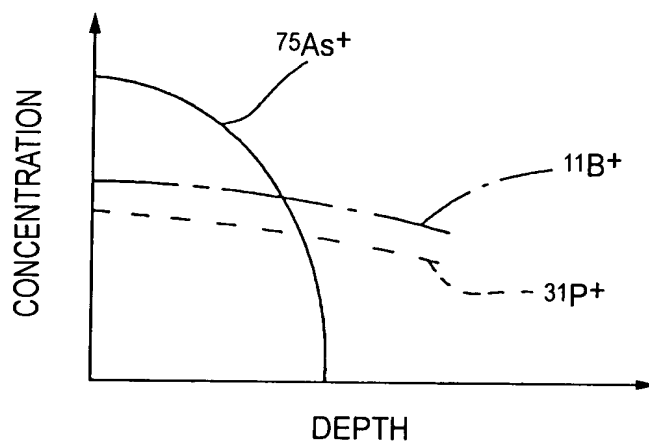


FIG. 6



The figure shows two cross-sectional views of a semiconductor device, labeled (A) and (B). Both views show a substrate 1 with a top layer 9. In view (A), there is a central region 5 with an N⁺ layer and an N⁻ layer. To the left of this region is a P⁺ layer 4 and an N⁺ layer 6. To the right is an N⁻ layer 9. A hatched region 7 is shown above the central region. A layer 12 is on the left. A layer 3 is on the far left. A layer 8 is on the right. A layer 21 is on the far right. A layer 22 is at the bottom. A layer 22A and 22B are also indicated. In view (B), the central region 5 is replaced by a P⁺ layer 56 and an N⁻ layer 57. The P⁺ layer 56 is further divided into regions 64A, 64B, and 64C. The N⁻ layer 57 is further divided into regions 65A, 65B, and 65C. The hatched region 7 is still present. The layer 12 is still on the left. The layer 3 is still on the far left. The layer 8 is still on the right. The layer 21 is still on the far right. The layer 22 is still at the bottom. The layer 22A and 22B are still indicated.

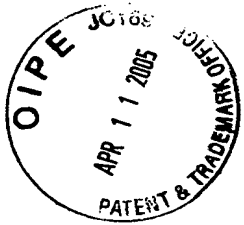
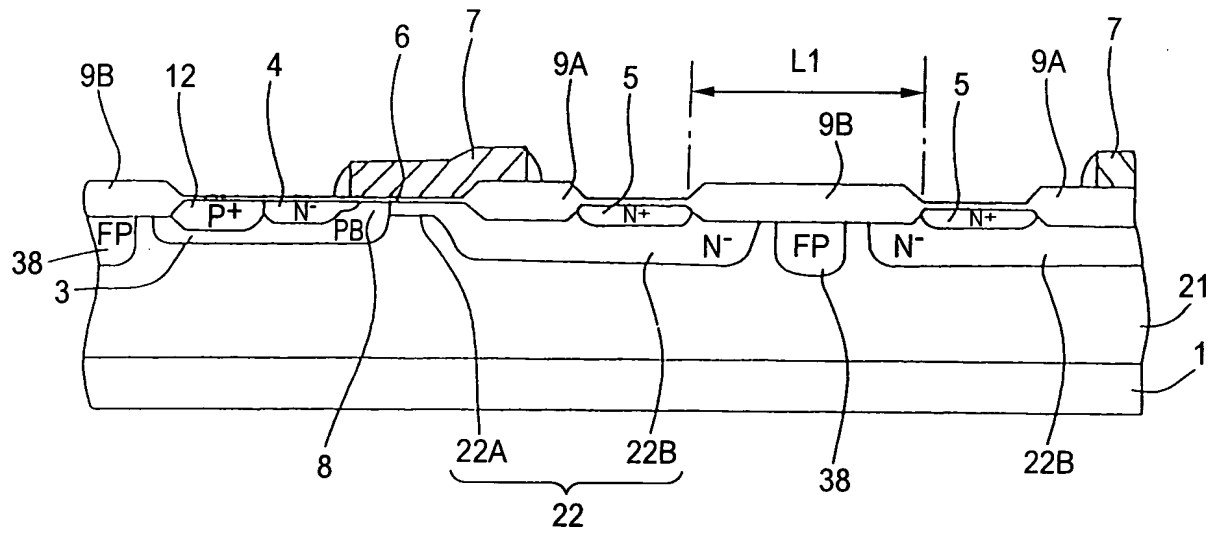


FIG. 8



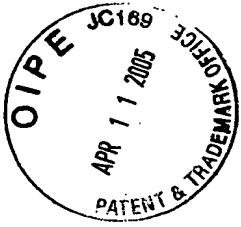
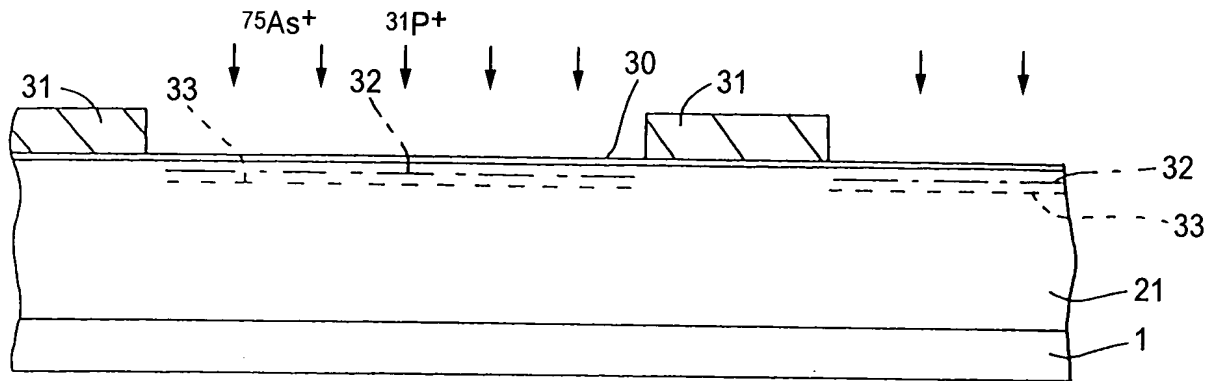


FIG. 9



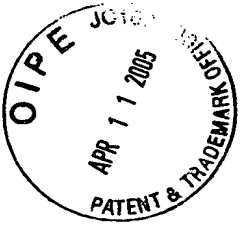
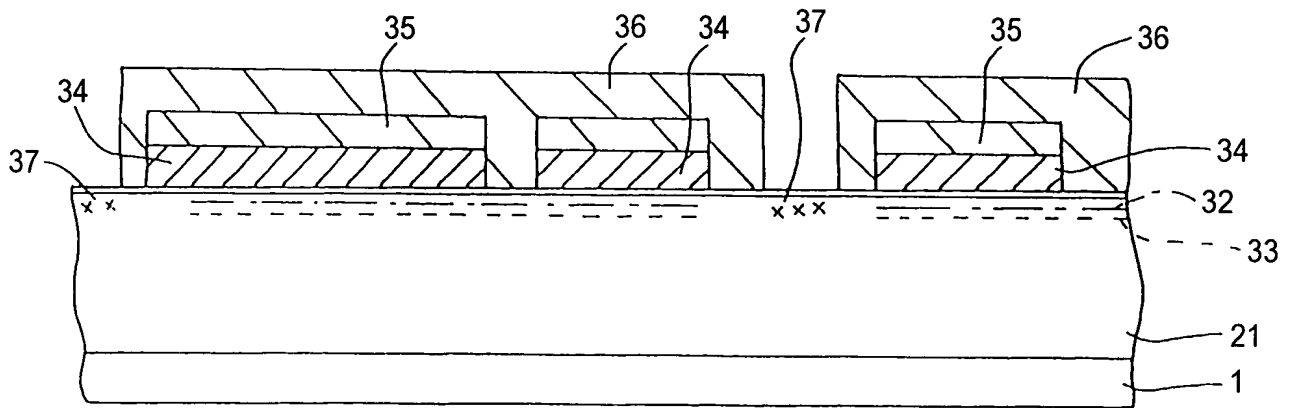


FIG. 10



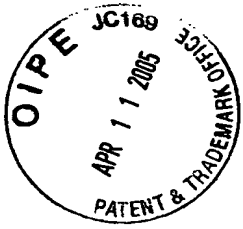
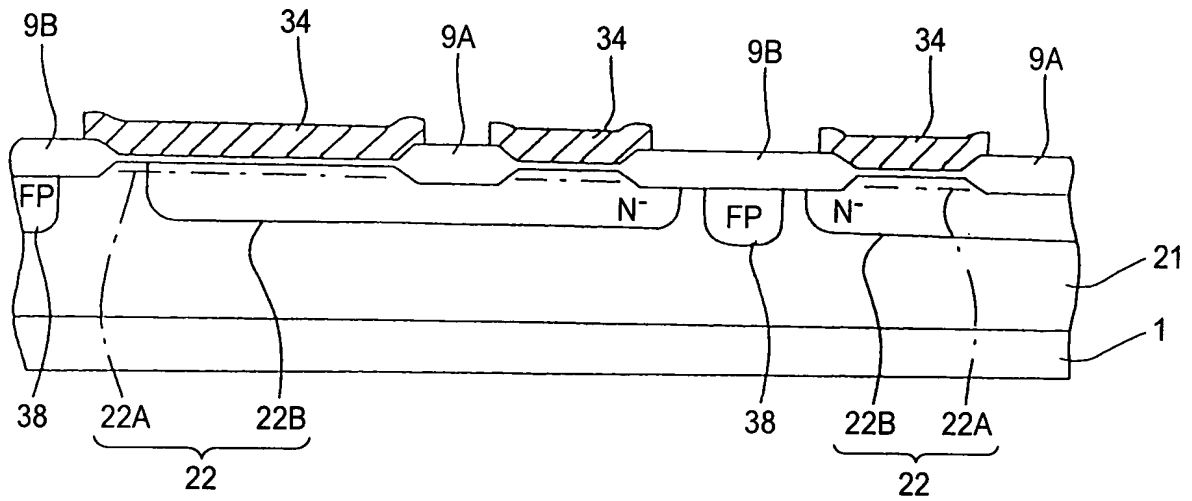


FIG. 11



[illegible]

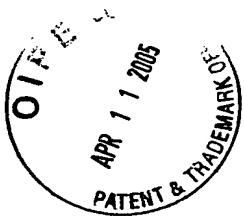
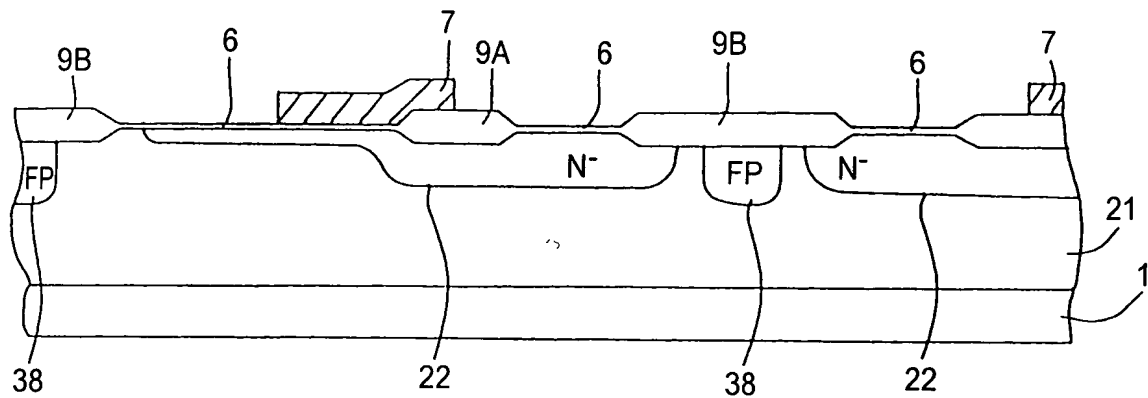


FIG. 13



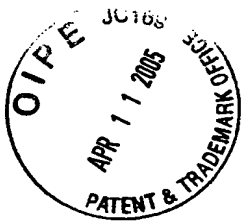
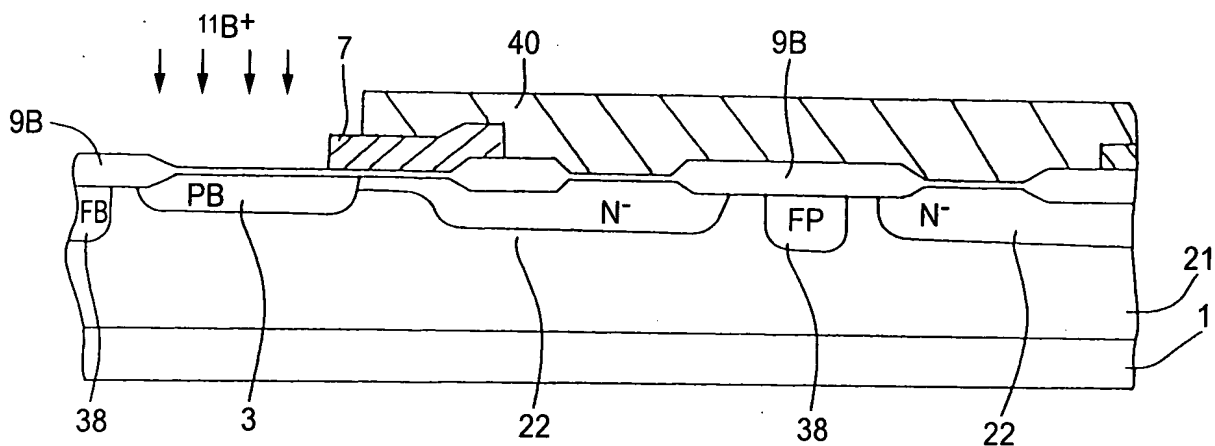


FIG. 14



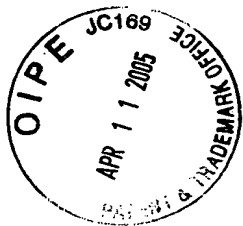
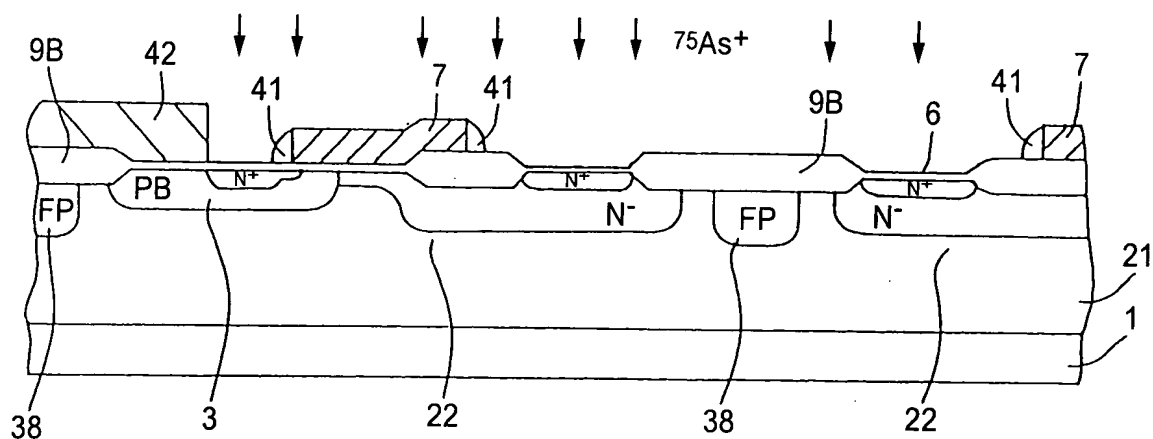


FIG. 15



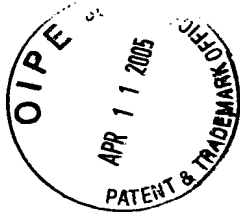
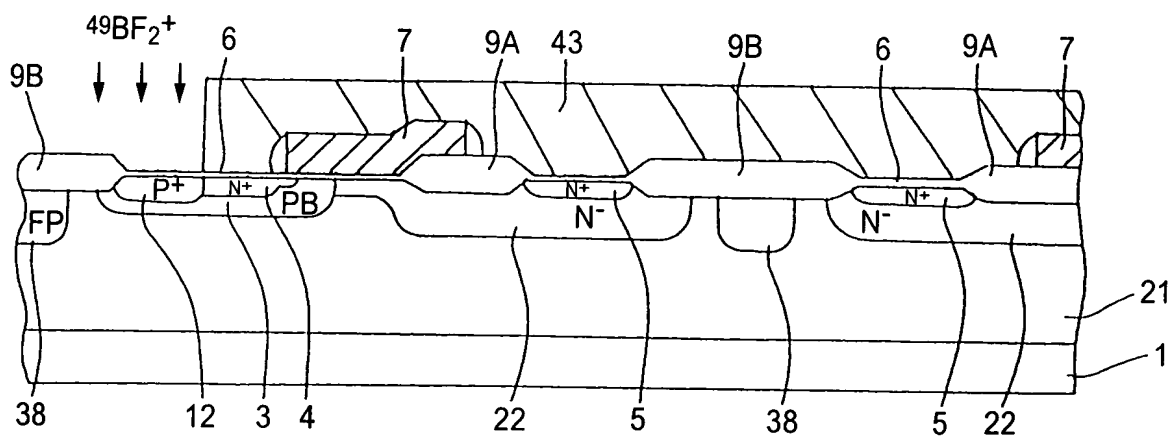
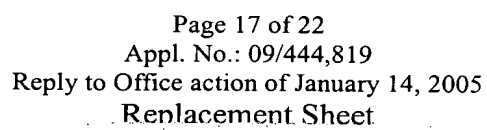


FIG. 16



[illegible]

[illegible]

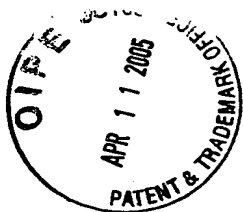


FIG. 19A

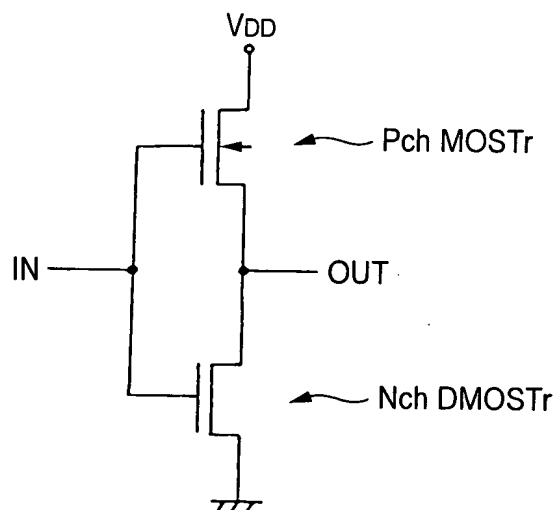
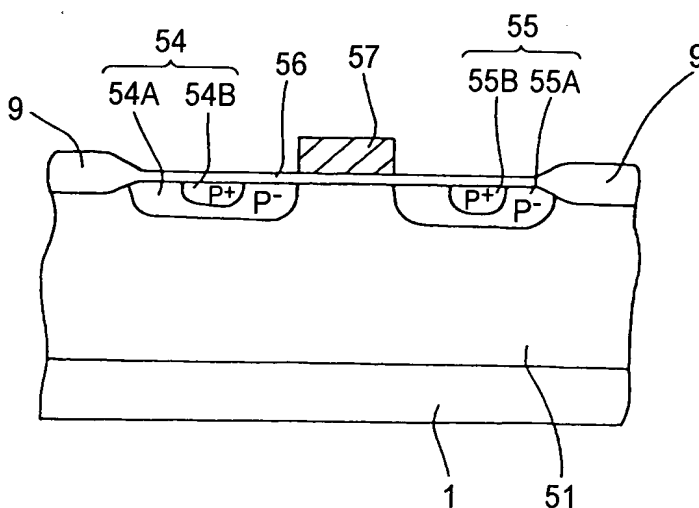


FIG. 19B



A detailed cross-sectional view of a semiconductor device, likely a MOSFET, showing two gate regions. The device is built on a substrate (1) with a thin layer (2). The left gate region (9A) has a gate stack (13) on top, a gate oxide (7), and a gate contact (G). Below the gate, there is a channel region (11) with an N+ dopant profile. The source (S) and drain (D) regions are formed in the substrate, with the source region (10) having a P+ dopant profile and the drain region (11) having an N+ dopant profile. A polysilicon layer (12) is present under the source region. A passivation layer (9B) covers the top of the device. The right gate region (9B) is similar but lacks the gate contact. A dimension line L2 indicates the length of the channel region. Various other components are labeled with numbers 1 through 13.

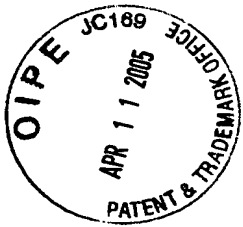


FIG. 21

N-CLAMP VOLTAGE VS. Na CONCENTRATION
STEPPED JUNCTION N-CONCENTRATION $1 \times 10^{17}/\text{cm}^3$
 $X_j = 0.2\mu\text{m}$

